

CLAIMS:

1. Mirror suppression circuit comprising a first quadrature signal path coupled between quadrature signal input and output terminals and including an error correction circuit for correction of amplitude and phase errors in a carrier modulated quadrature signal comprising a pair of in-phase and phase quadrature signal components, characterized by a quadrature output of said error correction circuit being coupled through a first filter circuit for a selection of said quadrature signal to a first quadrature input of an error detection circuit, said first quadrature signal path being coupled prior to said first filter circuit through a second quadrature signal path to a second quadrature input of said error detection circuit, said error detection circuit detecting amplitude and phase errors and providing amplitude and phase control signals to amplitude and phase control inputs of said error correction circuit for a negative feed back of said amplitude and phase errors to said error correction circuit, said amplitude control signal varying with at least one of products $I_w * I_{ref}$ and $Q_w * Q_{ref}$ and said phase control signal varying with at least one of products $I_w * Q_{ref}$ and $Q_w * I_{ref}$, I_w and Q_w , respectively I_{ref} and Q_{ref} , representing the in-phase and phase quadrature signal components of said quadrature signal at the first quadrature input of the error detection circuit, respectively the in-phase and phase quadrature signal components of a quadrature reference signal occurring at the negative carrier frequency of said quadrature signal at the second quadrature input of the error detection circuit.
2. Mirror suppression circuit according to claim 1, characterized by said amplitude control signal varying with $I_w * I_{ref} + Q_w * Q_{ref}$ and said phase control signal varying with $I_w * Q_{ref} - Q_w * I_{ref}$.
3. Mirror suppression circuit according to claim 1 or 2, characterized by the second quadrature signal path including inverter means providing signal inversion in obtaining said quadrature reference signal.

4. Mirror suppression circuit according to claim one of claims 1 to 3, characterized by said second quadrature signal path being coupled to the first quadrature signal path subsequent to the error correction circuit.
5. Mirror suppression circuit according to one of claims 1 to 4, characterized by said second quadrature signal path including a second filter circuit for a selection of said quadrature reference signal.
6. Mirror suppression circuit according to one of claims 3 to 5, characterized by said second quadrature signal path comprising said signal inverter coupled between the first quadrature signal path and said second filter circuit, said second filter circuit being identical to said first filter circuit.
7. Receiver providing quadrature signal processing comprising an RF input stage subsequently followed by a mixer stage for a conversion of an RF signal into an IF signal and an IF stage for a selective amplification of said IF signal, characterized by a mirror suppression circuit according to one of claims 1 to 5 having its quadrature signal input coupled to a quadrature output of the mixer stage and said first filter circuit being part of said IF stage and having a resonance frequency at the carrier frequency of said IF signal.
8. Receiver according to claim 7 comprising a mirror suppression circuit according to claim 5, characterized by the second filter circuit selecting said quadrature reference signal occurring at the negative carrier frequency of said quadrature IF signal.
9. Receiver according to claim 8 comprising a mirror suppression circuit according to claim 3, characterized by said second quadrature signal path comprising said signal inverter coupled between the first quadrature signal path and said second filter circuit, said second filter circuit being identical to said IF filter circuit.
10. Receiver according to claim 9, characterized by both first and second filter circuits comprising resonance amplifier type polyphase filters.

11. Receiver according to one of claims 1 to 10, characterized in that said error correction circuit includes an amplitude correction circuit comprising a first multiplier included in at least one of the pair of in-phase and quadrature paths of the first quadrature signal path for an amplitude variation of the signal at said input with said amplitude error.
12. Receiver according to claim 11, characterized by said amplitude correction circuit comprising a differential stage following said detection circuit converting said amplitude control signal into a differential pair of first and second amplitude control signals and supplying the same to said first and a second multiplier, respectively, said first and second multipliers being included in said in-phase and quadrature paths of the first quadrature signal path.
13. Receiver according to one of claims 1 to 10, characterized in that said error correction circuit includes a phase correction circuit comprising a third multiplier having a signal input coupled to one of said in-phase and quadrature paths of the first quadrature signal path and a signal output coupled to a first adder device, which is included in the other of said in-phase and quadrature paths for supplying thereto a part of the signal occurring at said one path to said other path varying with said phase control signal.
14. Receiver according to claim 13, characterized by said phase correction circuit comprising a differential stage following said detection circuit converting said phase error into a differential pair of first and second phase error signals and supplying the same to modulation signal inputs of said third and a fourth multiplier, respectively, said third and fourth multipliers having inputs coupled to the phase quadrature and in-phase paths of the first quadrature signal path and having outputs coupled to said first and a second adder device, which are included in said in-phase and phase quadrature paths, respectively.